IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Previously Presented): A semiconductor chip comprising:

a base substrate;

a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer, the bulk growth layer including a silicon bulk growth layer and a silicon germanium bulk growth layer;

a first isolation formed in the bulk device region so as to separate the bulk device;

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level;

a second isolation formed in the SOI device region so as to separate the SOI device; and

a boundary layer located at a boundary between the bulk device region and the SOI device region.

Claim 2 (Previously Presented): The semiconductor chip according to claim 1, wherein the boundary layer reaches the base substrate and is made of one of polysilicon or silicon-based compound semiconductors.

Claim 3 (Previously Presented): The semiconductor chip according to claim 1, wherein the first and second isolations are of substantially the same depth.

Claim 4 (Original): The semiconductor chip according to claim 3, wherein the first and second isolations have a depth reaching the buried insulator.

Claim 5 (Canceled).

Claim 6 (Previously Presented): The semiconductor chip according to claim 1, further comprising a third isolation positioned at the boundary and functioning as the boundary layer, wherein the first, second, and third isolations are of substantially the same depth.

Claim 7 (Currently Amended): A semiconductor chip comprising:

a base substrate;

a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer,

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level; and

a first isolation in the bulk device region, a second isolation in the SOI device region, and a third isolation positioned at a boundary between the bulk device region and the SOI device region and functioning as a boundary layer located at the boundary, the first, second, and third isolations being deeper than the buried insulator.

Claim 8 (Previously Presented): The semiconductor chip according to claim 7, wherein the third isolation has a sidewall that is in contact with the buried insulator.

Claim 9 (Previously Presented): The semiconductor chip according to claim 7, wherein the bulk device region has a pn junction positioned below an interface between the base substrate and the bulk growth layer.

Claim 10 (Previously Presented): The semiconductor chip according to claim 1, further comprising a third isolation positioned at the boundary and functioning as the boundary layer, wherein the second isolation is shallower than the third isolation.

Claim 11 (Previously Presented): The semiconductor chip according to claim 1, further comprising the first isolation in the bulk device region, and the second isolation that is shallower than the first isolation, wherein the boundary layer is whichever of the first or the second isolation that is positioned closest to the boundary.

Claim 12 (Previously Presented): The semiconductor chip according to claim 11, wherein the second isolation functions as the boundary layer, and has a bottom face that is in contact with the buried insulator.

Claim 13 (Original): The semiconductor chip according to claim 1, further comprising a dummy pattern in the bulk device region near the boundary.

Claim 14 (Previously Presented): A semiconductor chip comprising:

a base substrate;

a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device including a DRAM cell having a trench capacitor, is positioned on the bulk growth layer;

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level;

a boundary layer located at a boundary between the bulk device region and the SOI device region; and

a dummy pattern formed in the bulk device region near the boundary, the dummy pattern being a dummy capacitor.

Claim 15 (Original): The semiconductor chip according to claim 1, wherein the bulk device positioned in the bulk device region includes a DRAM cell having a trench capacitor, the trench capacitor comprising a first part extending at and below the interface between the base substrate and the bulk growth layer, and a second part extending above the interface, the width of the first part being greater than that of the second part.

Claims 16-28 (Canceled).

Claim 29 (Previously Presented): The semiconductor chip according to claim 1, wherein the bulk device positioned in the bulk device region includes a DRAM cell having a trench capacitor and a MOSFET, wherein the MOSFET is positioned between the DRAM cell and the boundary layer.

Claim 30 (Previously Presented): A semiconductor chip comprising:

a base substrate;

a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer, the bulk growth layer being a silicon germanium bulk growth layer;

a first isolation formed in the bulk device region so as to separate the bulk device;

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level;

a second isolation in the SOI device region so as to separate the SOI device; and

a boundary layer located at a boundary between the bulk device region and the SOI device region.

Claim 31 (Canceled).